







J176, J177 P-Channel JFET

Features

InterFET <u>P0099F Geometry</u>
 Low noise: 2.0 nV/vHz typical

· High gain: 10mS typical

· Low gate leakage: 2.5pA typical @10V

Typical loss: 10mATypical BVGss: -55VHigh radiation tolerance

• RoHS, REACH, CMR compliant

· Custom test and binning options available

· SMT, TH, and bare die package options

• SPICE Edge case modeling: InterFET SPICE

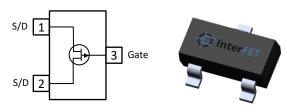
Industry Standard Crosses

SST176, SST177, 2N5116, SST270, SST271

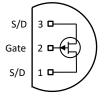
InterFET Similar Parts

- 2N5019, 2N5114, 2N5115, 2N5116
- P1086, P1087, J270, J271, VCR3P
- IFN3993, IFN3994, U304, U305, U306

SOT23 Top View



TO-92 Bottom View





NOTE: S/D pins are interchangeable Source Drain connections

Applications

- General: Amplifiers; Switches; Voltage regulators; Oscillators; Signal mixers; Noise generators
- · Military/Aero: Radar; Communications; Satellites; Missiles guidance; Hydrophone preamplifiers
- Medical: Medical imaging systems; Medical monitors and recorders; Ultrasound equipment
- · Audio: Tone control circuits; Headphone amplifiers; Audio filters; Electret Microphone

Description

The 30V InterFET J176 and J177 are very low leakage low noise P-channel JFETs targeted for high gain switching, commutator, and chopper applications. Gate leakages are typically less 3pA at room temperatures. The J177 has a cutoff voltage of less than 2.25V ideal for low-level power supplies. Proprietary InterFET processes yield exceptionally high radiation tolerance.

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J176; J177	Through-Hole	TO-92	Bulk
SMPJ176; SMPJ177	Surface Mount	SOT23	Bulk
	7" Tape and Reel: Max 3,000 Pieces		Minimum 1,000 Pieces
SMPJ176TR; SMPJ177TR	13" Tape and Reel: Max 9,000 Pieces	SOT23	Tape and Reel
J176COT; J177COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J176CFT; J177CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack









Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

	Parameters	SOT-23	TO-92	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-20	-20	V
I _{FG}	Continuous Forward Gate Current	50	50	mA
\mathbf{P}_{D}	Continuous Device Power Dissipation ¹	350	500	mW
Р	Power Derating ¹	2.8	4	mW/°C
TJ	Operating Junction Temperature	-55 to 150	-55 to 150	°C
Tstg	Storage Temperature	-55 to 150	-55 to 150	°C

¹ Thermal power dissipation and derating values obtained with gate pin (substrate) thermally connected to pad and/or internal layer.

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

			J176		J177		
	Parameters	Conditions	Min	Max	Min	Max	Unit
V _{(BR)GSS}	Gate to Source Breakdown Voltage	V _{DS} = 0V, I _G = 1μA	30		30		V
I _{GSS}	Gate to Source Reverse Current	V _{GS} = 20V, V _{DS} = 0V		1		1	nA
V _{GS(OFF)}	Gate to Source Cutoff Voltage	V _{DS} = -15V, I _D = -10nA	1	4	0.8	2.25	V
I _{DSS}	Drain to Source Saturation Current	$V_{GS} = 0V$, $V_{DS} = -15V$ (Pulsed)	-2	-35	-1.5	-20	mA
I _{D(OFF)}	Drain Cutoff Current	V _{DS} = -15V, V _{GS} = 10V		-1		-1	nA

Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

			J176		J177		
	Parameters	Conditions	Min	Max	Min	Max	Unit
R _{DS(ON)}	Drain to Source ON Resistance	V _{DS} <= 0.1V, V _{GS} = 0V, f = 1kHz		250		300	Ω
C _{gd}	Drain Gate Capacitance	V _{DS} = 0V, V _{GS} = 10V, f = 1MHz	5.5 (typ)		5.5 (typ)		рF
C _{gs}	Input Capacitance	V _{DS} = 0V, V _{GS} = 10V, f = 1MHz	5.5 (typ)		5.5 (typ)		pF
C _{gd} + C _{gs}	Drain + Source Gate Capacitance	V _{DS} = V _{GS} = 0V, f = 1MHz	32 (typ)		32 (typ)		pF
t _{d(ON)}	Turn ON Delay Time		15 (typ)	20 (typ)	ns
t _r	Rise Time	$V_{DD} = -6V$ $J176: V_{GS(OFF)} = 6V, R_L = 5600 \Omega$ $J177: V_{GS(OFF)} = 3V, R_L = 10000 \Omega$	20 (typ)		25 (typ)		ns
t _{d(OFF)}	Turn OFF Delay Time		15 (typ)		20 (typ)	ns
t _f	Fall Time		20 (typ)	25 (typ)	ns

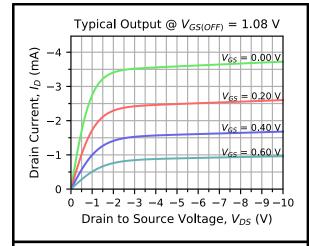


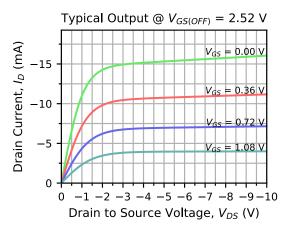


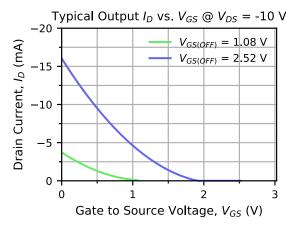


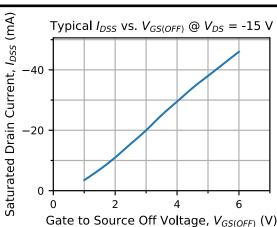


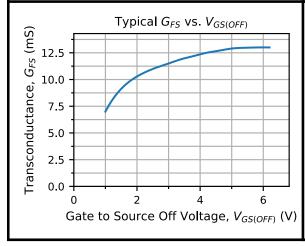
Typical J176, J177 Characteristics

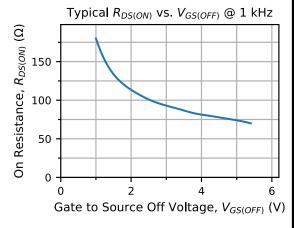












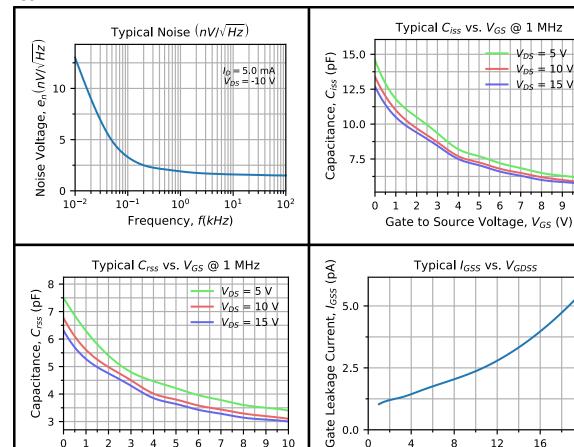








Typical J176, J177 Characteristics (Continued)



2 3 5 6

Gate to Source Voltage, V_{GS} (V)

8

8

Gate to Channel Voltage, V_{GDSS} (V)

12

16

20



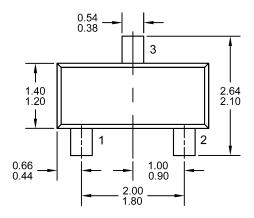


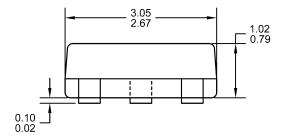


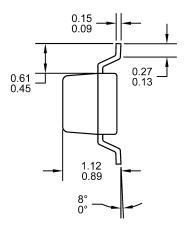


SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

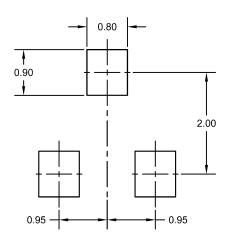






- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.12 grams
- 3. Molded plastic case UL 94V-0 rated
- For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
- Bulk product is shipped in standard ESD shipping material
- 6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



- 1. All linear dimensions are in millimeters.
- 2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.



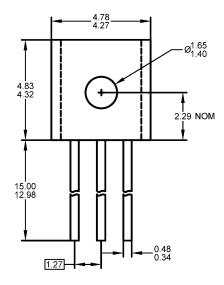


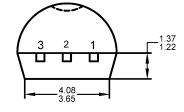


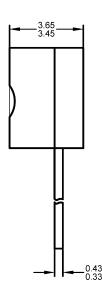


TO-92 Mechanical and Layout Data

Package Outline Data

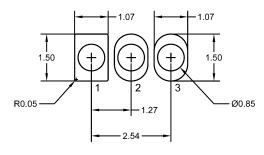






- 1. All linear dimensions are in millimeters.
- 2. Package weight approximately 0.19 grams
- 3. Molded plastic case UL 94V-0 rated
- Bulk product is shipped in standard ESD shipping material
- 5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



- 1. All linear dimensions are in millimeters.
- The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.









Compliance and Legal

Environment

InterFET parts follow the latest RoHS Compliance, REACH Compliance, Proposition 65 Statement, TSCA Statement, and Chemical Disposal and Waste Mitigation requirement and guidelines. For more on InterFET's Environmental Commitment please visit www.interFET.com/environmental/.

Package materials

Parameters	SOT23	SOIC8	TO-92	Metal Case
Alloy	CDA194	C194 1/2H	C194 1/2H	Kovar
Cu	Balance	97% min	97% min	
Fe	2.1 – 2.6%	2.1 – 2.6%	2.1 – 2.6%	53%
Zn	0.05 - 0.2%	0.05 - 0.2%	0.05 - 0.15%	
Р	0.015 - 0.15%	0.015 - 0.15%	0.015 - 0.15%	
Pb	0.03% max	0.03% max	0.03% max	
Ni				29%
Co				17%
Mn				0.3%
Si				0.2%
С				<0.01%
Au				Plating

Package tests

Parameters	rameters SOT23 SOIC8 TO-92		Metal Case	
MSL	Level 1	Level 2	N/A	N/A
ESD	Class M4 Machine Model	Class M4 Machine Model	Class M4 Machine Model	Class M4 Machine Model
	Class 3B HBM	Class 3B HBM	Class 3B HBM	Class 3B HBM

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