N-Channel Enhancement Mode Power MOSFET

Description

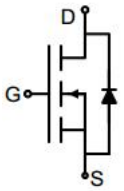
The GT060N04D3 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

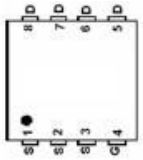
- V_{DS} 40V
- I_D (at V_{GS} = 10V) 56A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 8.5mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 11mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

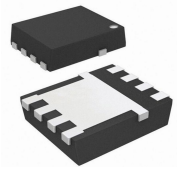
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



DFN3X3-8L

Ordering Information

Device	Package	Marking	Packaging
GT060N04D3	DFN3X3-8L	GT060N04	5000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Continuous Drain Current	I_D	56	A
Pulsed Drain Current (note1)	I_{DM}	224	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	60	W
Single pulse avalanche energy （note2）	E_{AS}	56	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	ºC/W
Maximum Junction-to-Case	R_{thJC}	2.08	ºC/W

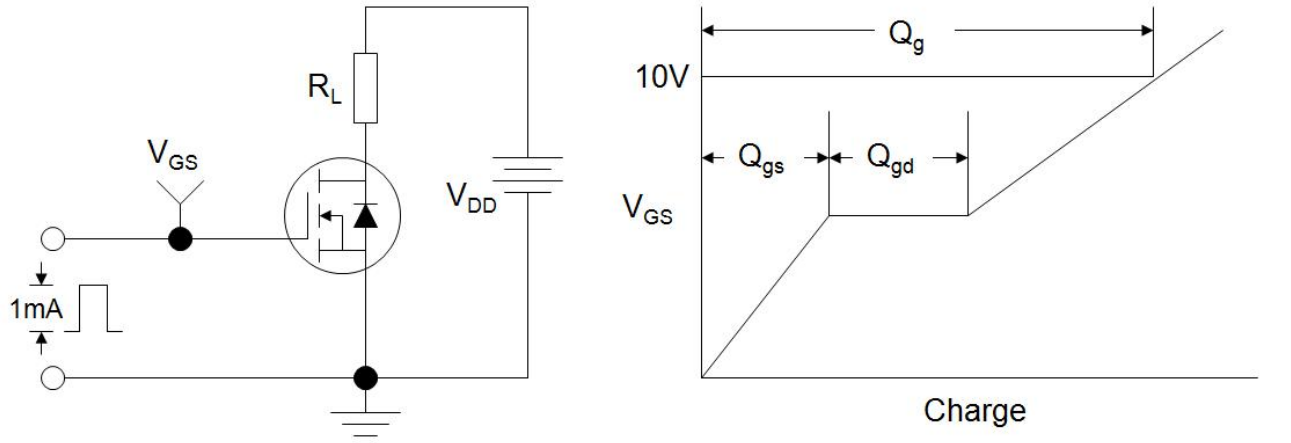
Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	40	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.8	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 30A	--	7	8.5	mΩ
		V_{GS} = 4.5V, I_D = 20A	--	9	11	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 15A	--	39	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 20V, f = 1.0MHz	--	1280	--	pF
Output Capacitance	C_{oss}		--	650	--	
Reverse Transfer Capacitance	C_{rss}		--	32	--	
Total Gate Charge	Q_g	V_{DD} = 20V, I_D = 30A, V_{GS} = 10V	--	25	--	nC
Gate-Source Charge	Q_{gs}		--	9	--	
Gate-Drain Charge	Q_{gd}		--	6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 20V, I_D = 30A, R_G = 3Ω	--	11	--	ns
Turn-on Rise Time	t_r		--	5	--	
Turn-off Delay Time	$t_{d(off)}$		--	26	--	
Turn-off Fall Time	t_f		--	5	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	56	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 30A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 30A, V_{GS} = 0V di/dt=100A/us	--	77	--	nC
Reverse Recovery Time	Trr		--	36	--	ns

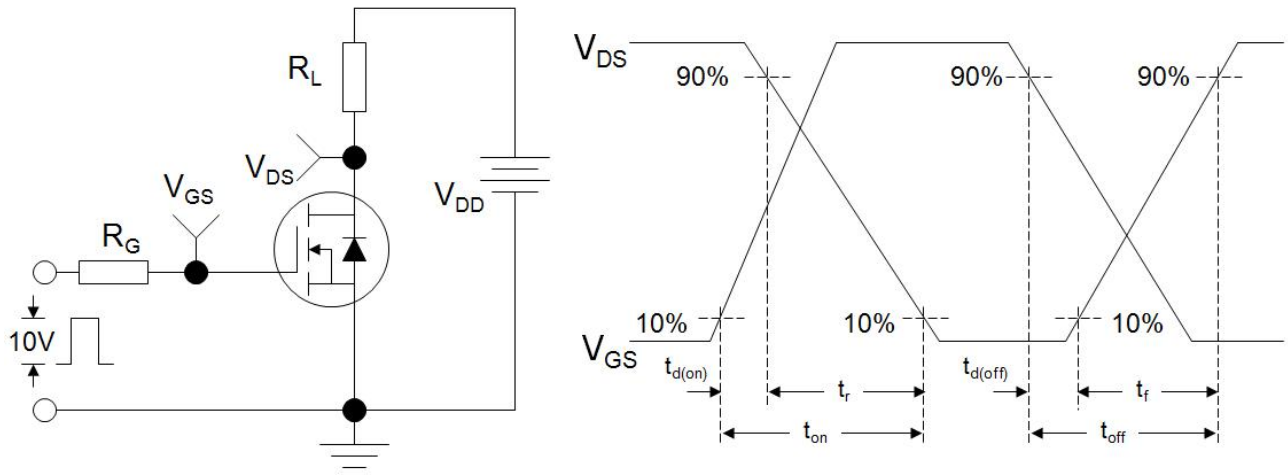
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=40V,VGS=10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 156mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

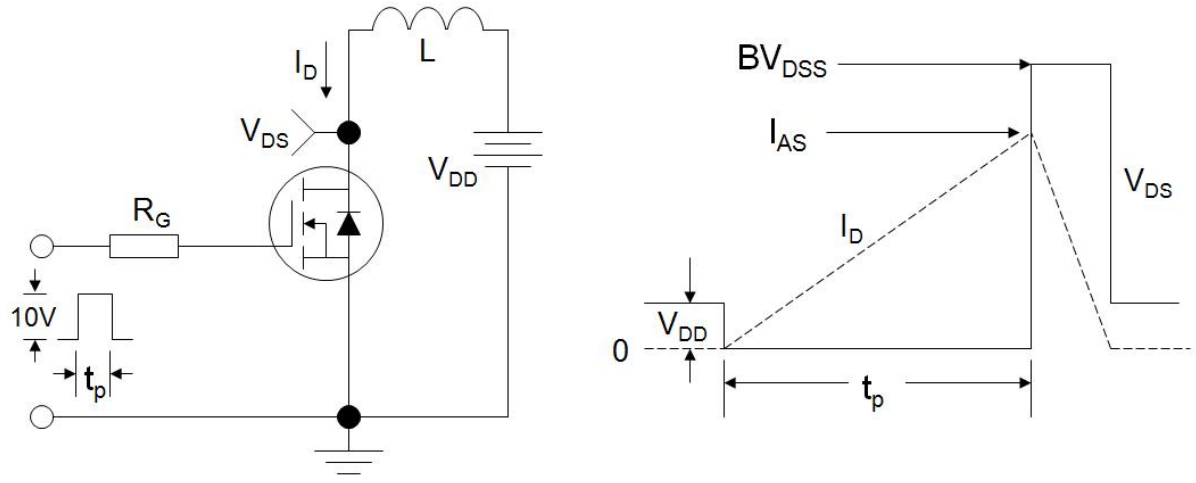
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

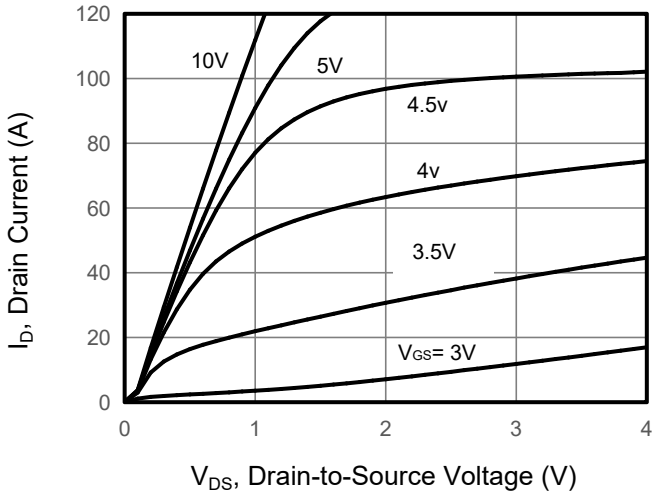


Figure 2. Transfer Characteristics

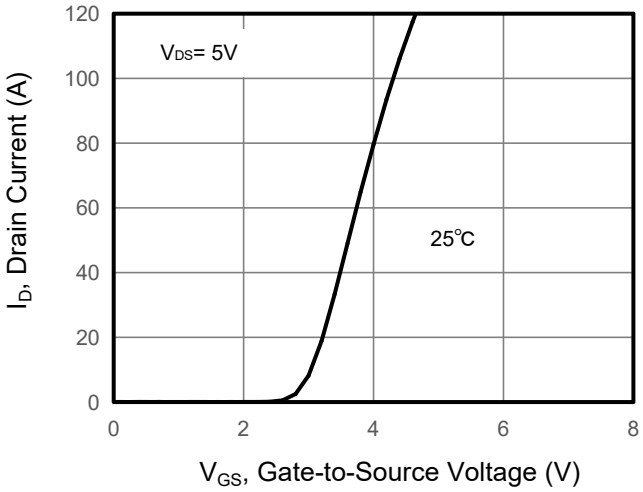


Figure 3. Drain Source On Resistance

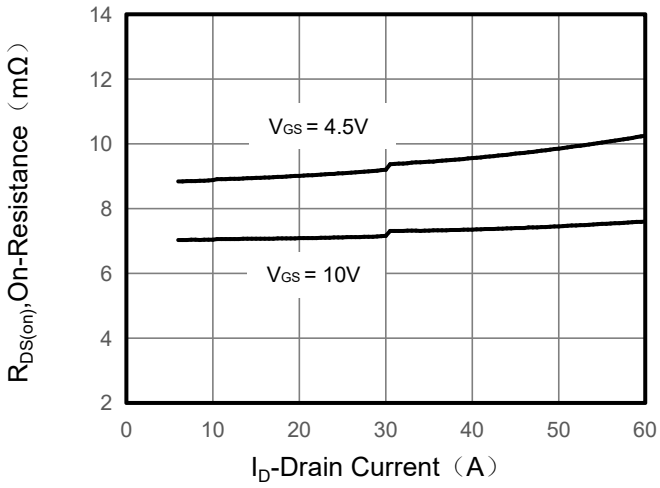


Figure 4. Gate Charge

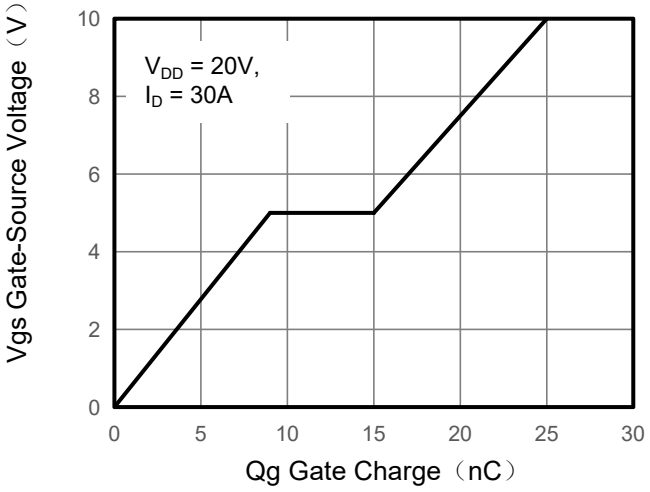


Figure 5. Capacitance

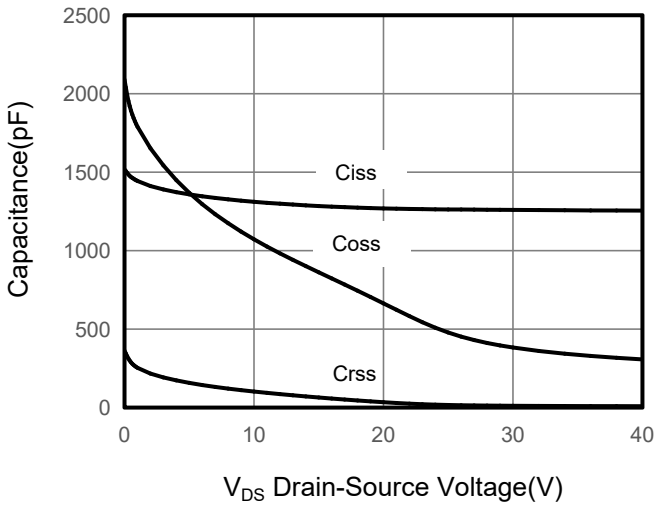
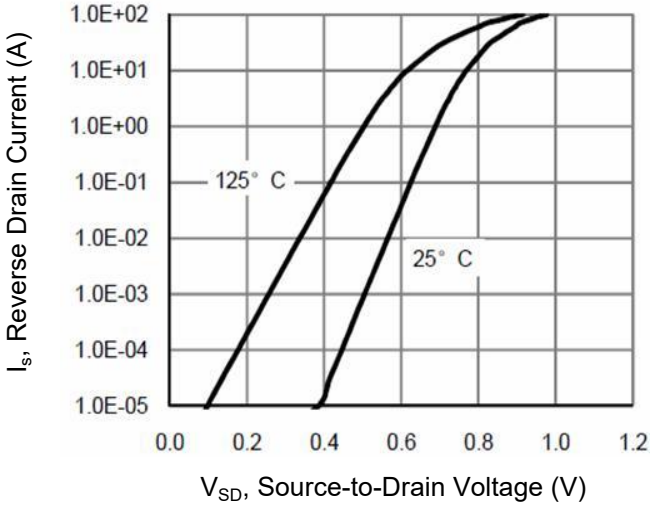


Figure 6. Source-Drain Diode Forward



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

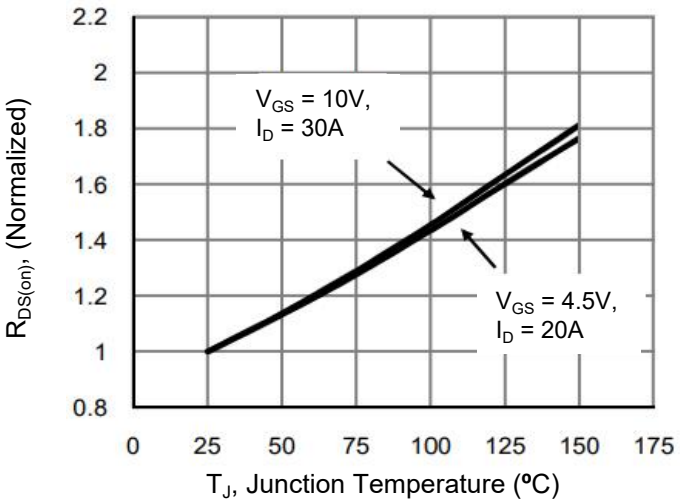


Figure 8. Safe Operation Area

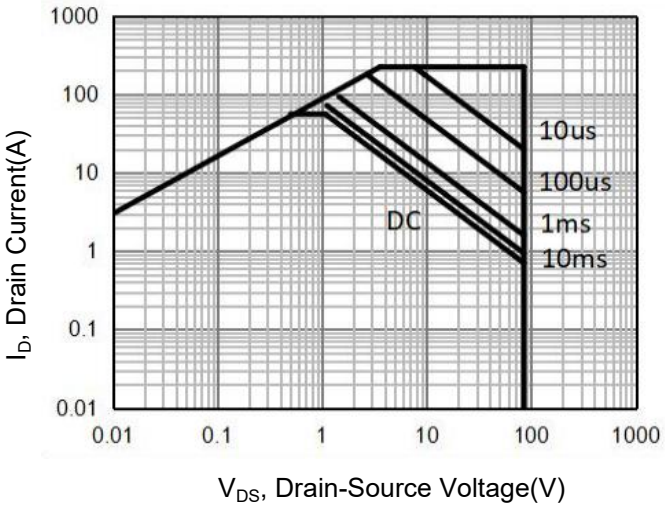
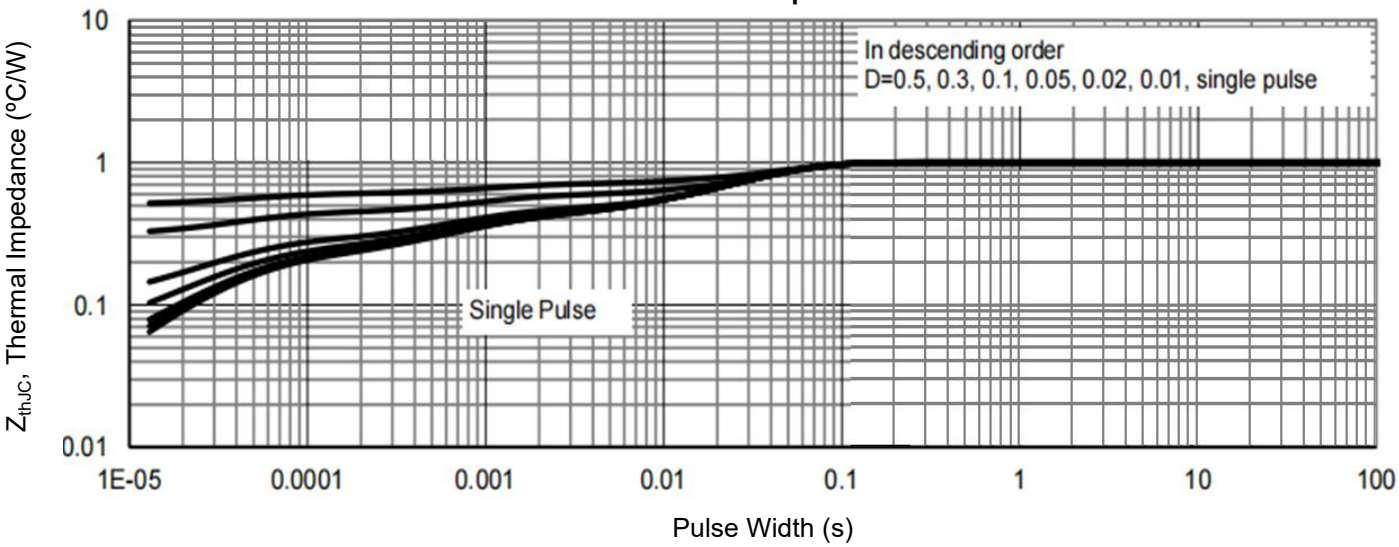
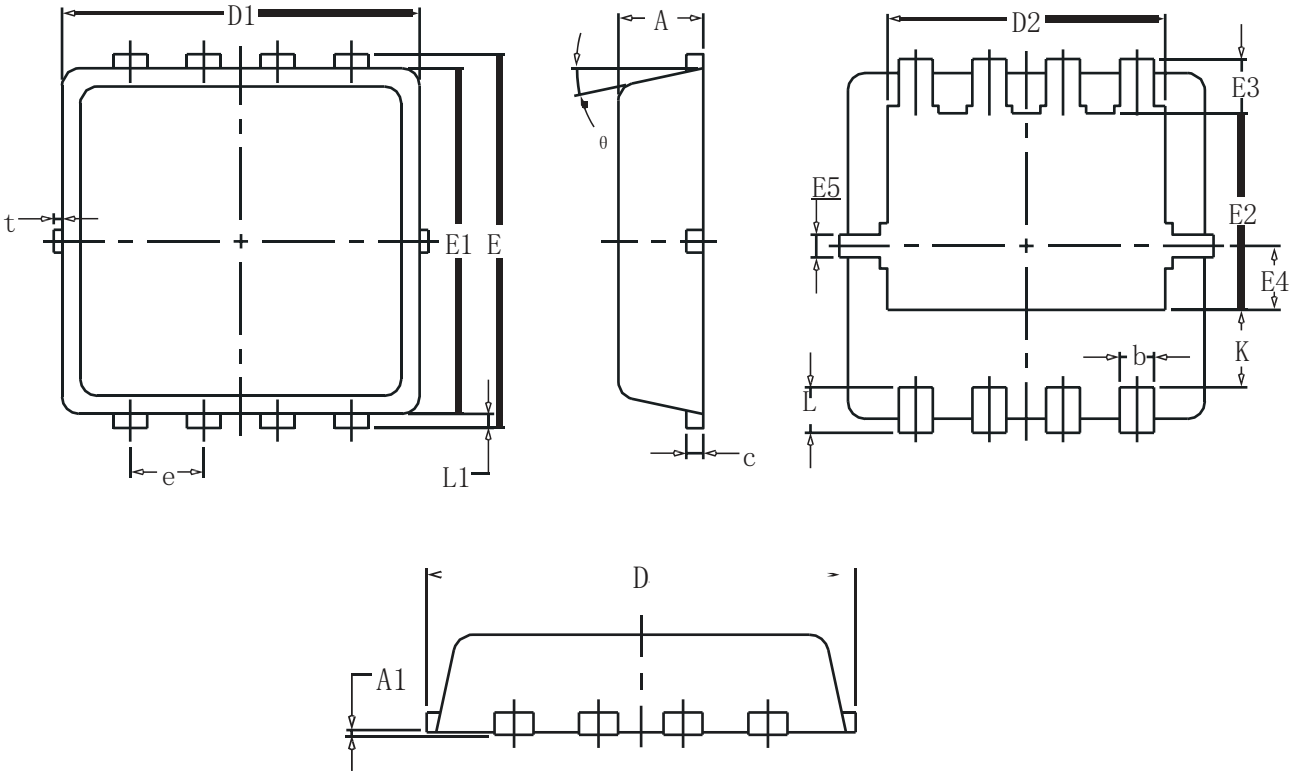


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN3x3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	-	-	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°