MT2201 - SD 3.0-SDR104 compliant integrated auto-direction control memory card voltage level translator with EMI filter and ESD protection

1. General description

The module is designed based on NVT4857UK produced by NXP Semiconductors (https://www.nxp.com/docs/en/data-sheet/NVT4857UK.pdf). It is an SD 3.0-compliant bidirectional dual voltage level translator with auto-direction control. It is designed to interface between a memory card operating at 1.8 V or 3.0 V signal levels and a host with a nominal supply voltage of 1.2 V to 1.8 V. The device supports SD 3.0 SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 High-Speed (50 MHz) and Default-Speed (25 MHz) modes. The device has an integrated voltage selectable low dropout regulator to supply the card-side I/Os, an auto-enable/ disable function connected to the VSD supply pin, built-in EMI filters and robust ESD protections (IEC 61000-4-2, level 4).

As shown in Fig. 1, the MT2201 converts the small BGA package NVT4857UK from 0.4 mm BGA to 1 mm pin pitch package to ease the PCB design and reduce the cost.

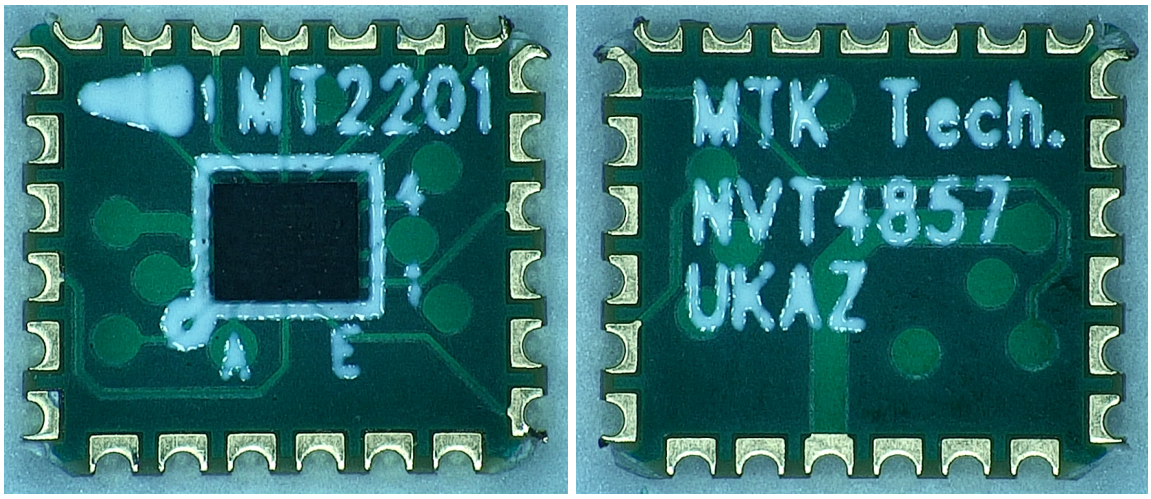


Fig.1 Top View (Left side) and Bottom View (Right side)

2. Features and benefits

a. Supports up to 208 MHz clock rate
b. SD 3.0 specification-compliant voltage translation to support SDR104, SDR50, DDR50, SDR25, SDR12, High-Speed and Default-Speed modes
c. 1.2 V to 1.8 V host side interface voltage support
d. Feedback channel for clock synchronization

e. 100 mA Low dropout voltage regulator to supply the card-side I/Os
f. Low power consumption by push-pull output stage with break-before-make architecture
g. Automatic enable and disable through VSD
h. Integrated pull-up and pull-down resistors: no external resistors required
i. Integrated EMI filters suppress higher harmonics of digital I/Os
j. Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on card side
k. Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
l. 25 pins four side; pitch 1 mm package

3. Applications

a. Xilinx FPGA such as ZYNQ US+/Versal
b. Altera FPGA SoC
c. Other large size SD card interface

4. Schematics

All 20 pins of NVT4857UK have been connected to MT2201 pins as shown in the Fig. 2.

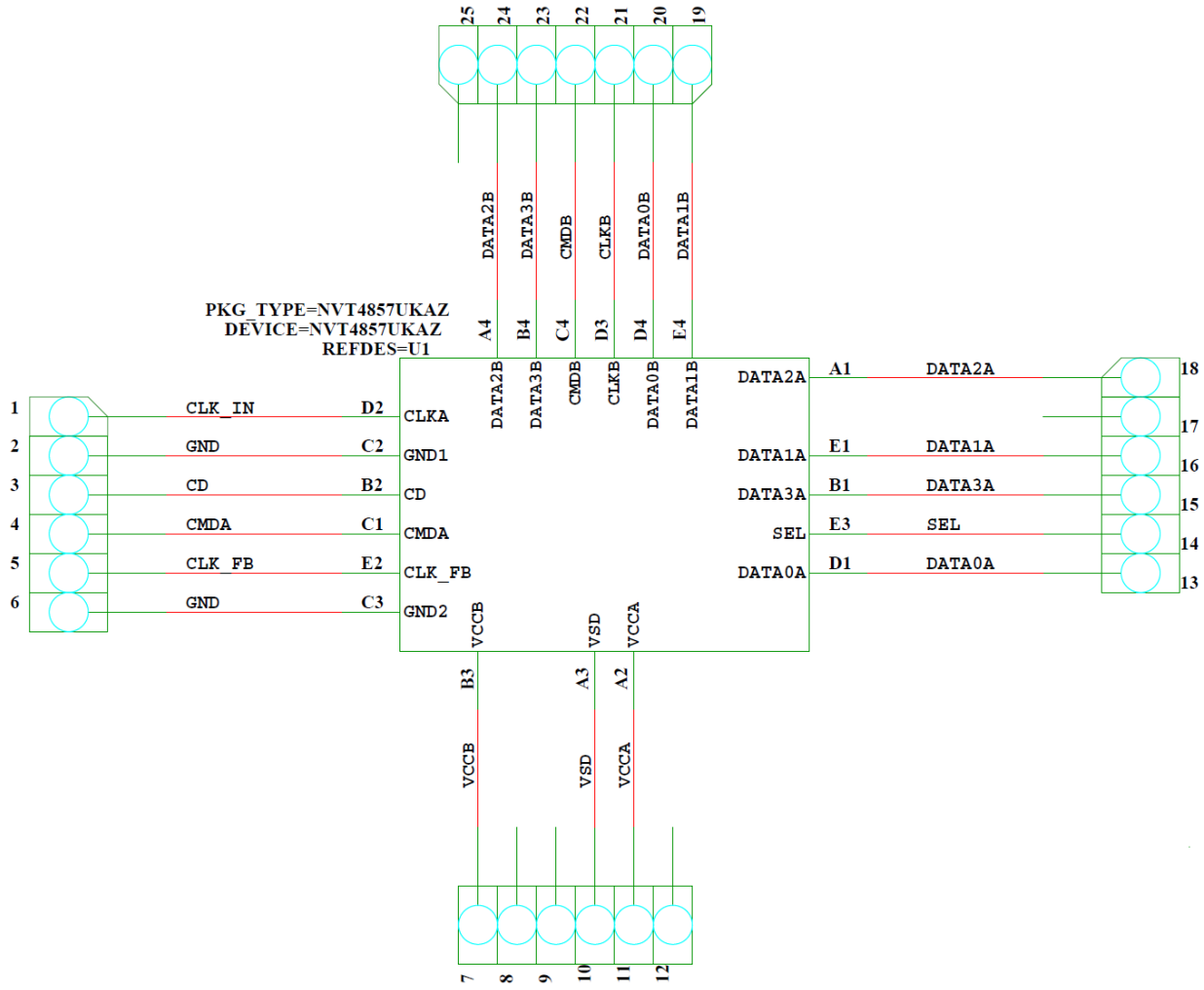


Fig. 2 MT2201 schematics

5. Pinning information

Table 1. Pin mapping and description

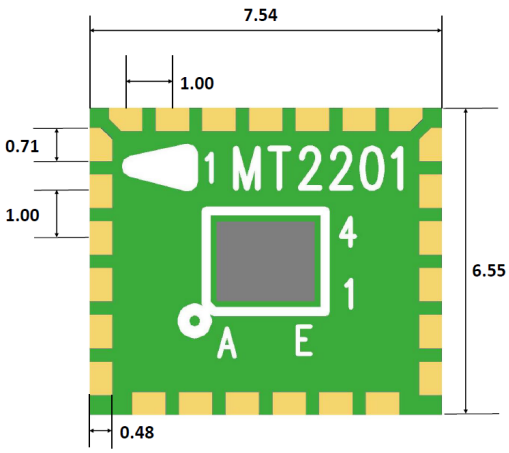
Pin Number	Pin Name	Type	Description
1	CLK_IN	Input	clock signal input on host side
2	GND	Power	power supply ground
3	CD	Output	card detect switch biasing output
4	CMDA	Input/Output	command input or output on host side
5	CLK_FB	Output	clock feedback output on host side

6	GND	Power	power supply ground
7	VCCB	Power	internal supply decoupling (VLDO)
8	NC	NC	Not Connected
9	NC	NC	Not Connected
10	VSD	Power	supply voltage
11	VCCA	Power	supply voltage from host side
12	NC	NC	Not Connected
13	DATA0A	Input/Output	data 0 input or output on host side
14	SEL	Input	card side I/O voltage level select
15	DATA3A	Input/Output	data 3 input or output on host side
16	DATA1A	Input/Output	data 1 input or output on host side
17	NC	NC	Not Connected
18	DATA2A	Input/Output	data 2 input or output on host side
19	DATA1B	Input/Output	data 1 input or output on memory card side
20	DATA0B	Input/Output	data 0 input or output on memory card side
21	CLKB	Output	clock signal output on memory card side
22	CMDB	Input/Output	command input or output on memory card side
23	DATA3B	Input/Output	data 3 input or output on memory card side
24	DATA2B	Input/Output	data 2 input or output on memory card side
25	NC	NC	Not Connected

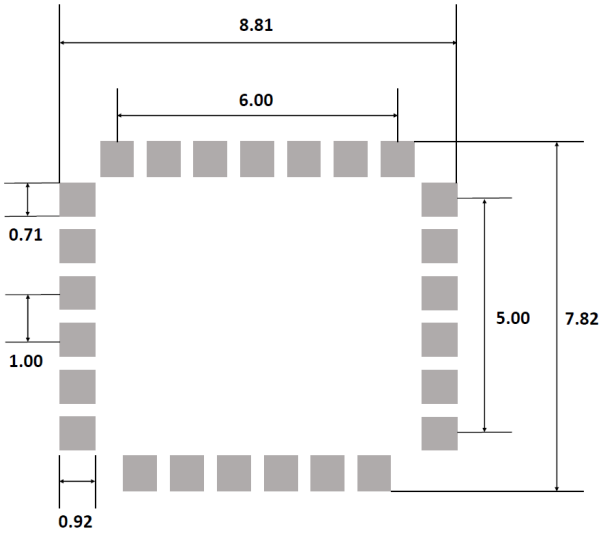
6. Functional description

Please refer to NVT4857UK Data Sheet for the details.
https://www.nxp.com/docs/en/data-sheet/NVT4857UK.pdf

7. Packing information



Size of the Component MT2201



Recommended Layout of MT2201

Note: All labels in this figure are in millimeters